A SIMD (Single Instruction Multiple Data) array processor is a type of computer processor that can execute a single instruction on multiple data elements simultaneously. SIMD processors are commonly used for vector operations, such as those required in image processing, audio processing, and scientific simulations.

The architecture of a SIMD array processor typically consists of several processing elements (PEs) that can operate in parallel. Each PE has its own local memory, and the PEs are interconnected in a regular array topology, typically a grid or mesh.

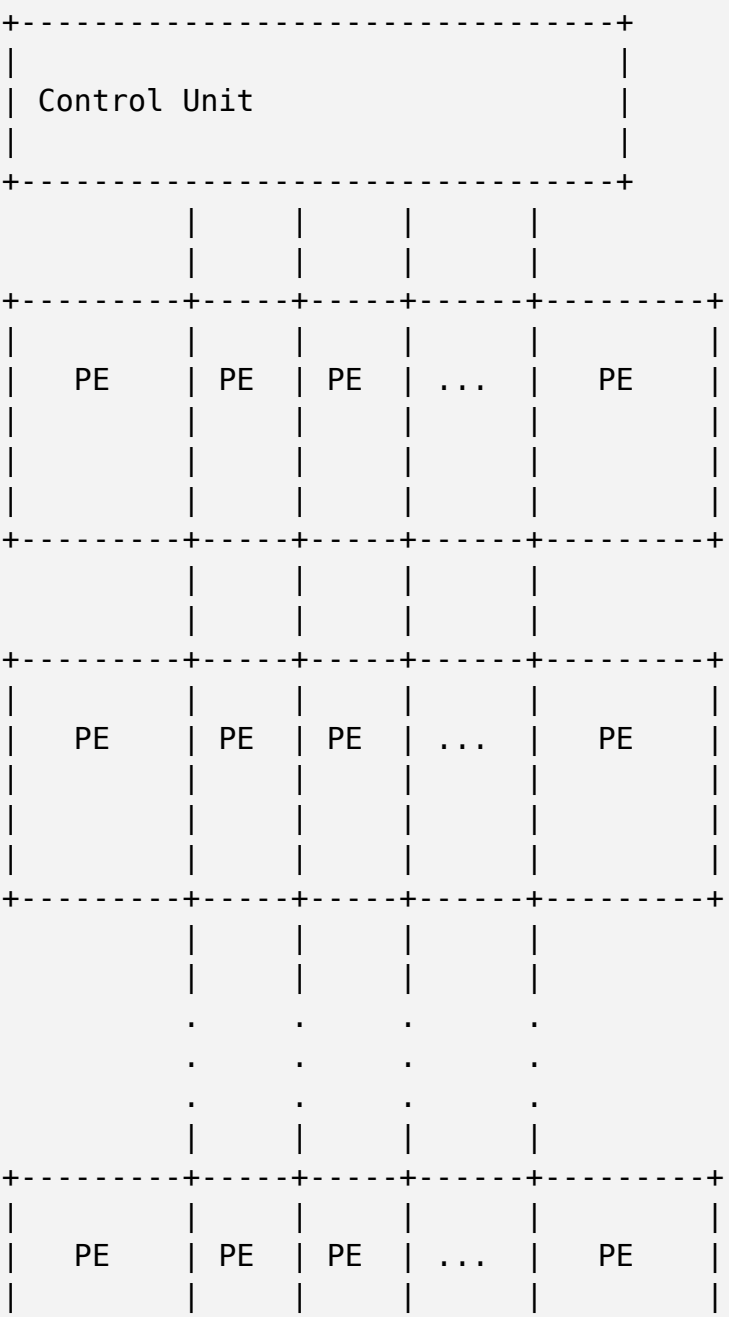
A typical SIMD array processor architecture consists of the following components:

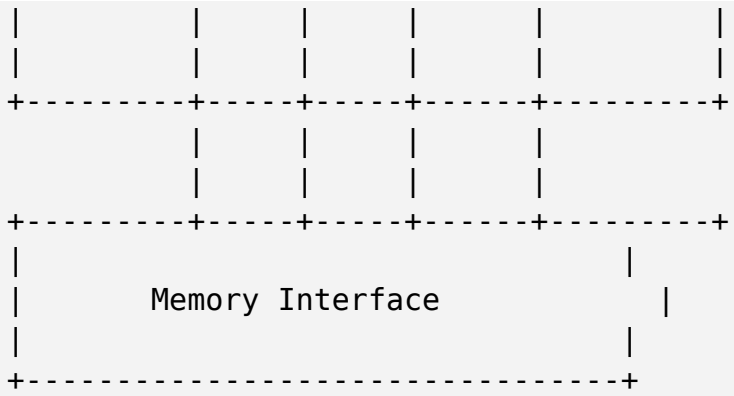
1. Control unit: The control unit generates the control signals that govern the operation of the processing elements. It also fetches instructions from memory and distributes them to the processing elements.
2. Processing elements (PEs): The processing elements are the computational units of the SIMD array processor. Each PE typically contains an arithmetic logic unit (ALU) and a local memory, which is used to store data and intermediate results.
3. Interconnect network: The interconnect network provides the communication infrastructure between the processing elements. It typically consists of a grid or mesh topology of buses or switches that allow PEs to communicate with each other.
4. Memory interface: The memory interface connects the SIMD array processor to external memory. It allows the processor to fetch data and instructions from memory and store results back to memory.

The architectural diagram of a SIMD array processor is shown

Explain SIMD array processor along with its architectural diagram ?

below:





In this diagram, the processing elements are arranged in a regular grid topology, with each PE having its own local memory. The control unit fetches instructions from memory and distributes them to the processing elements. The interconnect network provides the communication infrastructure between the processing elements, allowing them to exchange data

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22. What is the format of Micro Instruction in Computer Architecture explain ?
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36. Explain signed magnitude, signed l’s complement and signed 2’s complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.
37. If cache access time is lOOns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.
38. Explain hardwired microprogrammed control unit ? What is address sequencer circuit ?
39. Explain how a stack organized computer executes instructions? What is Stack?
40. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?
41. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
42. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
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44. Draw the functional and structural views of a computer system and explain in detail ?
45. Explain general register organization.
46. Compare and contrast DMA and I/O processors ?
47. Define the following: a) Flynn’s taxonomy b) Replacement algorithm
48. Explain the various pipeline vector processing methods ?
49. Describe the language features for parallelism ?
50. What are different addressing modes? Explain them.
51. Explain any page replacement algorithm with the help of example ?
52. What is mapping? Name all the types of cache mapping and explain anyone in detail.
53. Explain arithmetic pipeline ?
54. Write short notes on, a) SIMD, b) Matrix multiplication c) Instruction format
55. Differentiate: a) Maskable and non-maskable interrupt b) RISC and CISC
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Explain SIMD array processor along with its architectural diagram ?

57. Booths algorithm to muliyiply +5 and -15