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Explain hardwired microprogrammed control unit? What is address sequencer circuit?

A microprogrammed control unit (MCU) is a digital circuit that controls the operations of a computer's central processing unit (CPU).

There are two main types of MCUs:

- 1. Hardwired
- 2. Microprogrammed.

A hardwired control unit is a type of MCU that uses fixed, hardwired logic circuits to implement the control signals needed to execute instructions.

In this approach, the control unit's control signals are directly generated by the logic gates and flip-flops. This type of control unit is simple and fast, but it is difficult to modify or update once it is designed and implemented.

On the other hand, a microprogrammed control unit is a type of MCU that uses microcode to generate the control signals needed to execute instructions. In this approach, the control signals are stored in a memory called a control store, which can be easily modified or updated. This type of control unit is more flexible and easier to modify or update, but it is slower than a hardwired control unit.

An address sequencer circuit is a component of a microprogrammed control unit that generates the sequence of addresses that are used to read microinstructions from the control store. The address sequencer circuit typically consists of a counter and a decoder. The counter generates the addresses in sequence, while the decoder translates the addresses into the appropriate control signals that are used to fetch and execute instructions.

During the execution of an instruction, the address sequencer circuit generates a sequence

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of addresses that are used to read the corresponding microinstructions from the control store. Each microinstruction contains the control signals needed to execute a specific part of the instruction. The microinstructions are executed in sequence, with each microinstruction generating the control signals needed for the next step in the instruction execution process. Once all of the microinstructions for an instruction have been executed, the control unit generates the necessary signals to fetch the next instruction from memory, and the process repeats.

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- 19. Write a short note on design of arithmetic unit?
- 20. Write a short note on Array processors?
- 21. Write a short note on LRU algorithm?
- 22. What is the format of Micro Instruction in Computer Architecture explain?
- 23. What is the layout of pipelined instruction in Computer Architecture?
- 24. Explain the following interfaces in Detail:PCI Bus, SCSI Bus, USB Bus
- 25. What is Memory Organization? Discuss different types of Memory Organization in Computer System.
- 26. Computer Organization Q and A
- 27. Write short note on improving cache performance methods in detail?
- 28. What is Multiprocessor? Explain inter process communication in detail?
- 29. Briefly explain the concept of pipelining in detail?
- 30. Discuss the following in detail: RISC architecture, Vector processing?
- 31. Define the instruction format? Explain I/O System in detail?
- 32. Explain the design of arithmetic and logic unit by taking on example?
- 33. Explain how addition and subtraction are performed in fixed point number?
- 34. Explain different modes of data transfer between the central computer and I/O device ?
- 35. Differentiate between Serial and parallel data transfer?
- 36. Explain signed magnitude, signed I's complement and signed 2's complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.
- 37. If cache access time is IOOns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.
- 38. Explain how a stack organized computer executes instructions? What is Stack?
- 39. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?

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- 40. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
- 41. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
- 42. Explain SIMD array processor along with its architectural diagram?
- 43. Write short notes on
- 44. Draw the functional and structural views of a computer system and explain in detail?
- 45. Explain general register organization.
- 46. Compare and contrast DMA and I/O processors?
- 47. Define the following: a) Flynn's taxonomy b) Replacement algorithm
- 48. Explain the various pipeline vector processing methods?
- 49. Describe the language features for parallelism?
- 50. What are different addressing modes? Explain them.
- 51. Explain any page replacement algorithm with the help of example?
- 52. What is mapping? Name all the types of cache mapping and explain anyone in detail.
- 53. Explain arithmetic pipeline?
- 54. Write short notes on, a) SIMD, b) Matrix multiplication c) Instruction format
- 55. Differentiate: a) Maskable and non-maskable interrupt b) RISC and CISC
- 56. Computer Organization Previous Years Solved Questions
- 57. Booths algorithm to muliyiply +5 and -15