In computer architecture, general register organization refers to the way in which registers are organized and used within a CPU. Registers are small, high-speed storage locations within the CPU that are used for storing data that is being operated on.

The general register organization typically consists of a set of general-purpose registers that can be used for a variety of purposes, such as storing operands for arithmetic operations, holding data for memory access, and storing intermediate results during instruction execution. The number and size of the registers vary depending on the CPU architecture.

A common organization for general registers is to have a set of registers that are dedicated to specific purposes, such as holding the program counter (PC), the stack pointer (SP), and the base pointer (BP). In addition to these dedicated registers, there is typically a set of general-purpose registers that can be used for a variety of purposes.

For example, the x86 architecture used in many personal computers has eight general-purpose registers, labeled as EAX, EBX, ECX, EDX, ESI, EDI, EBP, and ESP. These registers are each 32 bits in size and can be used for a variety of purposes.

The MIPS architecture used in many embedded systems has 32 general-purpose registers, labeled as $0 to $31. These registers are each 32 bits in size and are used for a variety of purposes, such as holding operands for arithmetic operations, holding pointers to memory locations, and storing intermediate results during instruction execution.

The organization and use of general registers can have a significant impact on CPU performance. By having a sufficient number of registers and using them efficiently, CPU designers can reduce the need to access main memory for data storage and retrieval, which can improve overall system performance.

Explain general register organization.

Related Posts:

1. Structure of Desktop computers
2. Logic Gates
3. Register Organization
4. Bus structure in Computer Organization
5. Addressing modes
6. Register Transfer Language
7. Numerical problem on Direct mapping
8. Registers in Assembly Language Programming
9. Array in Assembly Language Programming
10. Net 31
11. How to start with GNU Simulator 8085
12. Cache Updating Scheme
13. Cache Memory
14. Principle of Cache Memory
15. Cache Mapping
16. Addition and subtraction in fixed point numbers
17. PCI Bus
18. Booths Algorithm
19. Write a short note on design of arithmetic unit ?
20. Write a short note on Array processors ?
21. Write a short note on LRU algorithm ?
22. What is the format of Micro Instruction in Computer Architecture explain ?
23. What is the layout of pipelined instruction in Computer Architecture ?
24. Explain the following interfaces in Detail:PCI Bus, SCSI Bus, USB Bus
25. What is Memory Organization ? Discuss different types of Memory Organization in Computer System.

26. Computer Organization Q and A
27. Write short note on improving cache performance methods in detail ?
28. What is Multiprocessor ? Explain inter process communication in detail ?
29. Briefly explain the concept of pipelining in detail ?
30. Discuss the following in detail: RISC architecture, Vector processing ?
31. Define the instruction format ? Explain I/O System in detail ?
32. Explain the design of arithmetic and logic unit by taking on example ?
33. Explain how addition and subtraction are performed in fixed point number ?
34. Explain different modes of data transfer between the central computer and I/O device ?
35. Differentiate between Serial and parallel data transfer ?
36. Explain signed magnitude, signed l's complement and signed 2's complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.
37. If cache access time is lOOns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.
38. Explain hardwired microprogrammed control unit ? What is address sequencer circuit ?
39. Explain how a stack organized computer executes instructions? What is Stack?
40. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?
41. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
42. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
43. Explain SIMD array processor along with its architectural diagram ?
44. Write short notes on
45. Draw the functional and structural views of a computer system and explain in detail ?

46. Compare and contrast DMA and I/O processors ?
47. Define the following: a) Flynn’s taxonomy b) Replacement algorithm
48. Explain the various pipeline vector processing methods ?
49. Describe the language features for parallelism ?
50. What are different addressing modes? Explain them.
51. Explain any page replacement algorithm with the help of example ?
52. What is mapping? Name all the types of cache mapping and explain anyone in detail.
53. Explain arithmetic pipeline ?
54. Write short notes on, a) SIMD, b) Matrix multiplication c) Instruction format
55. Differentiate: a) Maskable and non-maskable interrupt b) RISC and CISC
56. Computer Organization Previous Years Solved Questions
57. Booths algorithm to muliyiply +5 and -15