CBSE NET July 2016 PAPER II

Q. In a Positive edge triggered JK flip-flop, if J and K both are high then the output will be _____ on the rising edge of the clock.

(A) No change
(B) Set
(C) Reset
(D) Toggle

Ans :- (D)

Explanation:-
State table of JK Flip Flop –

J	K	OUTPUT
0	0	No change
0	1	0
1	0	1
1	1	Toggle

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69. Write a short note on design of arithmetic unit ?
70. Write a short note on Array processors ?
71. Write a short note on LRU algorithm ?
72. What is the format of Micro Instruction in Computer Architecture explain ?
73. What is the layout of pipelined instruction in Computer Architecture ?
74. Explain the following interfaces in Detail:PCI Bus, SCSI Bus, USB Bus
75. What is Memory Organization ? Discuss different types of Memory Organization in Computer System.
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77. Write short note on improving cache performance methods in detail ?
78. What is Multiprocessor ? Explain inter process communication in detail ?
79. Briefly explain the concept of pipelining in detail ?
80. Discuss the following in detail: RISC architecture, Vector processing ?
81. Define the instruction format ? Explain I/O System in detail ?
82. Explain the design of arithmetic and logic unit by taking on example ?
83. Explain how addition and subtraction are performed in fixed point number ?
84. Explain different modes of data transfer between the central computer and I/O device

?

85. Differentiate between Serial and parallel data transfer ?
86. Explain signed magnitude, signed l's complement and signed 2's complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.
87. If cache access time is lOOns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.
88. Explain hardwired microprogrammed control unit ? What is address sequencer circuit ?
89. Explain how a stack organized computer executes instructions? What is Stack?
90. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?
91. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
92. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
93. Explain SIMD array processor along with its architectural diagram ?
94. Write short notes on
95. Draw the functional and structural views of a computer system and explain in detail ?
96. Explain general register organization.
97. Compare and contrast DMA and I/O processors ?
98. Define the following: a) Flynn's taxonomy b) Replacement algorithm
99. Explain the various pipeline vector processing methods ?
100. Describe the language features for parallelism ?
101. What are different addressing modes? Explain them.
102. Explain any page replacement algorithm with the help of example ?
103. What is mapping? Name all the types of cache mapping and explain anyone in detail.
104. Explain arithmetic pipeline ?

105. Write short notes on, a) SIMD, b) Matrix multiplication c) Instruction format
106. Differentiate: a) Maskable and non-maskable interrupt b) RISC and CISC
107. Computer Organization Previous Years Solved Questions
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